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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,936	11/28/2001	Sadashige Sugiura	60188-121	7332

20277 7590 07/16/2003

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EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,936	SUGIURA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *2 and 6-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *15 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. This application claims priority under 35 U.S.C. 119 based on priority application serial No. 2000-360526, filed on November 28, 2000, in Japan.

Election/Restriction

2. Claims 2 and 6-12 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, in view of the previous office action, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 9.

Accordingly, claims 1-12 are pending in this application; and claims 1 and 3-5 remain active in this Office action.

Drawings

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on May 15, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3, as being best understood in view of the above objections to the claims and to the specification, are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi et al. ("Nakanishi"; US 5,110,664).

Nakanishi discloses a semiconductor device (See Fig. 1), comprising: a semiconductor wiring substrate (17, 37 and 18) including a plurality of wires (13 and 29); a IC chip (1), which is regarded here as inherently having intellectual property and including a circuit having semiconductor device elements arranged therein; and at least one test pad (3) connected to at least one of the wires of the semiconductor wiring substrate. It is noted that the test pad (3) in Nakanishi is inherently capable of functioning as a test pad for testing an electrical connection between the circuit of the chip and the wires, as it is a test pad and electrically connected to both of the circuit and the wires.

Regarding claim 3, the test pad in Nakanishi is a portion of the at least one of the wires that is exposed on a surface of the semiconductor wiring substrate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5, as being best understood in view of the above objections to the claims and to the specification, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. ("Nakanishi"; US 5,110,664) in view of Voldman (US 5,625,280).

The disclosure of Nakanishi is discussed as applied to clams 1 and 3 above.

Nakanishi does not expressly disclose that the circuit in the chip can have a diode connected to a power supply line and a node and then to two test pads. However, one of ordinary skill in the art would readily recognize that a circuit in a chip can be protected by a diode, as evidenced in Voldman. Voldman (see Figs. 1-3, and col. 5, lines 19-24) teaches to protect a circuit from ESD damages by connecting a protection diode (27 or 28) between a node (26) and a line (a power supply line10; or a ground line 13), wherein the node and the line are connected respectively to pads (26) and 11 (or the bottom left one).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pad-connected protection diode of Voldman into the device of Nakanishi, so that a semiconductor device with better chip protection would be obtained.

Response to Arguments

6. Applicant's arguments filed on 5/15/03 have been fully considered but they are not persuasive.

Applicant's main arguments include: (A) Nakanishi does not anticipate the claimed invention, because Nakanishi is silent as to how the test pad 3 would be used to test electrical connections between the substrate wiring and the chip; and (B) There is no suggestion to combine the applied references.

With respect to applicant's Argument A above, it is noted that the test pad 3 in Nakanishi is a test pad that is electrically connected to both of the circuit in the chip and the wirings in the substrate; and such a test pad is inherently for test the electrical properties of the circuit in the chip through the wirings (see particularly Fig. 1, and col. 6, lines 31-35). Accordingly; the test of the electrical connection between the circuit of the chip and the wirings would be the least such an electrical test pad has to be able to function, otherwise the test pad would not be able to test anything else about the chip. Therefore, the test pad 3 in Nakanishi inherently functions to test the electrical connection between the circuit of the chip and the wires.

In addition, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "test pins", "quick and easy testing mechanism") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding applicant's Argument B that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, although Nakanishi does not expressly disclose that the circuit in the chip can have a diode connected to a power supply line and a node and then to two test pads, one of ordinary skill in the art would readily recognize that a circuit in a chip can be protected by such a diode connection. And, such knowledge and desirability are generally available to one of ordinary skill in the art, as evidenced in Voldman. Voldman (see Figs. 1-3, and col. 5, lines 19-24) teaches to protect a circuit from ESD damages by connecting a protection diode (27 or 28) between a node (26) and a line (a power supply line10; or a ground line 13), wherein the node and the line are connected respectively to pads (26) and 11 (or the bottom left one). It would therefore well within the ordinary skill in the art at the time the invention was made to incorporate the pad-connected protection diode of Voldman into the device of Nakanishi for forming a semiconductor device with better chip protection.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
July 15, 2003

Shouxiang Hu
Patent Examiner
TC 2800